Notice of References Cited	Application/Control No. 10/676,890	Applicant(s)/Patent Under Reexamination JEYASINGH ET AL.	
	Examiner Gopal C. Ray	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,812,967	03-1989	Hirosawa et al.	710/269
*	B	US-5,452,462	09-1995	Matsuura et al.	718/1
*	C	US-6,870,899	03-2005	Lu et al.	379/1.04
*	D	US-2005/0210467	09-2005	Zimmer et al.	718/001
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Test floor verification of multiprocessor hardware" by Saha et al. (abstract only) Publication Date: 27-29 March 1996
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.